Exhibit 4

[redacted]

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case No. IPR2022-00062
U.S. Patent No. 9,858,218

NETLIST, INC.'S PATENT OWNER'S PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit Number	Description
2001	Declaration of Robert J. Murphy, dated February 18, 2022
2002	Deposition of Dr. Donald Alpert, IPR2020-01044, *SK hynix, Inc., et al. v. Netlist, Inc.*, dated March 10, 2021
2003	Deposition of Dr. Donald Alpert, IPR2018-00303, *SK hynix, Inc., et al. v. Netlist, Inc.*, dated July 20, 2018
2004	U.S. Patent Publication No. 2005/0138267 to Bains *et al.*
2005	U.S. Patent No. 7,870,459 to Hazelzet
2006	IT Solution Architects, *Server Memory: RDIMM vs LRDIMM and When to Use Them* (Aug. 16, 2017), https://medium.com/@ITsolutions/server-memory-rdimm-vs-lrdimm-and-when-to-use-them-a550f4b7cf39
2007	U.S. Patent No. 8,402,208 to Berke
2008	U.S. Patent No. 8,452,917 to Amer *et al.*
2009	U.S. Patent Publication No. 2011/0007585 to Shan *et al.*
2010	U.S. Patent No. 8,054,664 to Harashima *et al.*
2011	Excerpt of *DRAM Circuit Design, Fundamental and High-Speed Topics* (2008)
2012	Excerpt of *Semiconductor Memories, A Handbook of Design, Manufacture, and Application Second Edition* (1997)
2013	JEDEC, *Member Online Services*, https://www.jedec.org/service_members/
2014	JEDEC, *Membership Details*, https://www.jedec.org/join-jedec/
2015	U.S. Patent Publication No. 2005/0138302 to Lusk *et al.*

Exhibit Number	Description
2016	Intel, *Fully Buffered DIMM (FB-DIMM) Design Considerations* (Feb 18, 2004), http://www.csit-sun.pub.ro/~cpop/Documentatie_SMP/Intel_Microprocessor_Systems/PC_Memory/OSA-S009.pdf
2017	Microway, *DDR4 RDIMM and LRDIMM Performance Comparison* (July 10, 2015), https://www.microway.com/hpc-tech-tips/ddr4-rdimm-lrdimm-performance-comparison/
2018	U.S. Patent Publication No. 2009/0103373 to Shau
2019	Redline comparison of 2022IPR-00062 to IPR2020-01044
2020	Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 9,858,218, dated June 8, 2020 (Exhibit 1003 to IPR2020-01044)
2021	U.S. Patent No. 10,474,595 to Lee

I. Introduction

Petitioner largely reiterates arguments made by SK Hynix in the prior IPR proceeding concerning US Patent No. 9,858,218 ("the '218 patent"), where IPR was instituted and the parties settled shortly thereafter. *SK Hynix Inc. et al v. Netlist, Inc.* PTAB-IPR2020-01044. However, this Patent Owner's Preliminary Response presents evidence and arguments not presented or considered by the Board during that prior institution decision.

For example, this Preliminary Response explains how JEDEC (EX1015)—extensively relied on by Petitioner—is not a "printed publication" and therefore not prior art. Additionally, this Preliminary Response further explains how the claims of the '218 patent are fully supported by the provisional application that predates JEDEC, and that Petitioner's own arguments confirm this. This Preliminary Response also explains why Petitioner's proposed combinations are further deficient because, after institution in the prior IPR, Petitioner's own expert admitted that the proposed combination here would be ***inoperable***, removing any motivation POSITA would have used to combine them in the first place. Finally, as explained here, the Board could—and should—use its discretion to deny institution.

II. Overview of the '218 Patent

The '218 patent has a priority date of June 12, 2009, and relates to the operation of memory modules. EX1001. The '218 patent discloses a memory module that can perform two types of operations, e.g., initialization operation, during which the memory module is initialized or trained with one or more initialization or training sequences, and normal memory operation, during which the memory module is accessed for normal memory read or write operations. The '218 patent further discloses that the memory module can communicate a "notification signal" to a host system such as a system memory controller associated with the one or more initialization or training sequences. EX1001, Abstract.

The '218 patent describes an elegant solution using existing hardware to create a new way for the memory module to communicate with a system memory controller during initialization/training. At the time of the '218 patent, "[e]xisting initialization schemes [had] certain inefficiencies which [led] to wasted time and expense." EX1001, 2:49-50. This was primarily because there was no existing method for a memory subsystem (e.g., memory module) to communicate to the MCH (e.g., system memory controller) during initialization. *Id.*, 2:59-65. Prior art methods included the MCH "polling" the memory module to determine whether training was complete, or simply waiting a pre-determined period of time, based on an estimation of when the module controller would have completed the training

sequence. *Id.*, 3:30-58. Both methods were inefficient because the system memory controller did not know when training was complete. *Id.*, 3:13-58.

The '218 patent provides a solution whereby the memory module may use existing hardware to signal the system memory controller during initialization/training, e.g., to "notify" the MCH when training is complete. *Id.*, 3:59-4:18. This was unprecedented because, prior to the invention, memory modules had always been *reactive* components, meaning that signals sent by a memory module were *in response to* a command or signals received from the host system. In contrast, the '218 patent's memory module is *active*, *initiating contact* with the host system by outputting to the host system a signal associated with training sequences. *Id.*, 1:45-49, 1:66-2:2, 2:20-24, 4:31-37, 7:2-14. Such signaling "can be an open drain signaling from the memory subsystem controller to the MCH" and uses an open-drain output that already exists on the memory module. *Id.*, 4:1-18.

The '218 Patent memory modules can have both a "first mode" and a "second mode." *Id.*, 1:42-52, 1:63-2:8, 2:9-14, 4:24-28, 5:61-64, 7:58-65, 9:20-24, 11:47-51, 12:13-17, 12:44-48. In the first mode, the memory module executes training and is not accessed by the host for read or write operations. *Id.*, 1:45-49, 2:17-24, 4:24-31, 5:61-6:10, 6:15-30, 7:3-18, 9:20-27, 11:46-54, 11:55-63. In the second mode, the memory module performs standard operations (e.g., read or write operations) in

response to read or write commands from the host system. *Id.*, 1:49-58, 2:2-6, 6:41-48, 12:4-8.

III. Claim Constructions

Patent Owner does not respond here to Petitioner's proposed claim constructions (Pet. Section V.D) because, even under Petitioner's proposals, the Board should deny institution. This Preliminary Response should not be interpreted as agreement with Petitioner's proposals, and Patent Owner reserves the right to offer competing construction if institution is granted.

IV. Overview of References

1. Hazelzet

U.S. Patent App. Pub. No. 2008/0098277 to **Hazelzet** (EX1014) was filed on October 23, 2006. Hazelzet discloses a memory module including error correction code (ECC) logic "to identify and correct single bit errors on the command or address bus." EX1014, [0008]. Hazelzet includes an error reporting mode during which the system can interrogate the module regarding its error status. *Id.*, [0009]. Hazelzet implements these features in a register "having error correction code (ECC), parity checking, a multi-byte fault reporting register, read via an independent bus, and real time error lines for both correctable errors and uncorrectable error conditions." *Id.*, [0016]. Thus, Hazelzet discloses a hybrid device utilizing error detection, error correction, and parity. It does not include memory buffers that buffer

the data lines and it does not discuss or mention memory buffer training. EX2001, ¶50.

2. JEDEC

The **JEDEC Proposal** (EX1015) (or "**JEDEC**") is not prior art to the '218 patent because it post-dates the priority date of the '218 Patent. *See infra* Section VI. The '218 patent claims priority to Provisional Application No. 61/186,799 (EX1008, 12) ("Priority Application") which has a filing date of June 12, 2009. EX1001. Nonetheless, JEDEC discloses Write Leveling and Read Enable Training for an LRDIMM including memory buffers (MB). EX1015, 4. JEDEC states that the MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training. EX1015, 8; EX2001, ¶52.

3. Buchmann

U.S. Patent No. 8,139,430 to **Buchmann** (EX1016) discloses a power-on initialization test for a cascade interconnect system. Buchmann discloses a memory buffer including a bus interface to links in a high-speed channel for communicating with a memory controller via a direct connection or via a cascade interconnection and another memory buffer. EX1016, 1:39-44. The interface is operable in a static-bit-communication (SBC) mode and a high-speed mode. *Id.* The memory buffer includes logic for executing a power-on and initialization training sequence initiated

by the memory controller. *Id.*, 1:44-48. The sequence is for initializing the links to the high-speed channel. EX1016, 1:48-50; EX2001, ¶51. Buchmann teaches that the SBC is used for handshaking between the memory buffers in the cascade. EX1016, 5:47-49.

V. Ground 1 Should be Denied Because JEDEC Is Not a Publicly Accessible Printed Publication

JEDEC is not a "printed publication." A petition may be instituted "only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b); *Regents of the Univ. of Minn. v. LSI Corp.*, 926 F.3d 1327, 1335 (Fed. Cir. 2019). A reference qualifies as a "printed publication" under section 102(a) only if is it "publicly accessible." *Jazz Pharms., Inc. v. Amneal Pharms., LLC*, 895 F.3d 1347, 1355 (Fed. Cir. 2018). Petitioner bears the burden of demonstrating public accessibility. *Id.*, 1356.

Petitioner claims that JEDEC is "publicly accessible" because it was distributed to members of a particular JEDEC committee and was subsequently accessible to POSITA. Pet., 26. To carry its burden, Petitioner had to prove both that (1) the JEDEC Proposal was available to POSITA (and not just those who were already JEDEC members) and (2) that POSITA could reasonably have found the Proposal. *Samsung Electronics Co. Ltd. v. Rembrandt Wireless Technologies, LP,*

IPR2014-00514, Paper 18, at 4 (P.T.A.B. Sept. 9, 2014)) ("*Rembrandt* Final Written Decision"); *SRI Int'l, Inc. v. Internet Sec. Sys., Inc.*, 511 F.3d 1186, 1196 (Fed. Cir. 2008). Petitioner failed to carry its burden as to either requirement.

First, the Petition is bereft of any explanation of how anyone who was not a member of the JC.40.4 subcommittee before November 11, 2009, would know that the JEDEC Proposal existed, let alone be able to access it. Petitioner makes no showing that anyone outside of the JC-40.4 subcommittee knew about the JEDEC Proposal. *SRI,* 511 F.3d at 1196 (reference distributed within SRI was not publicly available because "only one non-SRI person ... specifically knew about the availability of the [reference]"); *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1349 (Fed. Cir. 2016) (reference not publicly available because "there was no evidence that the ordinarily skilled artisan would know of" the website where the reference was hosted).

Instead, Petitioner relies on "a letter ballot" that was distributed to members of the JEDEC JC-40.4 subcommittee on November 11, 2009, which contained a "link" to the JEDEC Proposal. Pet., 26. Although Petitioner claims that the letter ballot was distributed without an expectation of confidentiality, Petitioner proffers no evidence that any member actually further distributed the Proposal. *Id.*, 26-27; *e.g.*, *Nokia Corp. v. Ipcom*, No. IPR2021-00533, 2021 WL 3575135, at *12 (P.T.A.B. Aug. 12, 2021) (merely disseminating a "meeting report" that "attached

[a] list of technical documents" including standards proposal did not make the proposal publicly available). Nor has Petitioner shown that POSITA would be independently aware of JEDEC letter ballots (such as the JEDEC Proposal) at all, particularly because they are only available to members of that specific subcommittee. EX2013; *see SRI,* 511 F.3d at 1196.

Petitioner's position here is the same as that rejected by the Board in *Samsung v. Rembrandt*, where institution turned on whether a draft IEEE standard was a "printed publication." *Rembrandt* Final Written Decision at 4. There, Samsung argued that the reference was uploaded to an IEEE working-group server available to IEEE members, advertised on a publicly accessible listserv, and accessible to "any interested parties." *Id*., 5-7. But the Board denied institution, concluding that the reference was *not* publicly accessible because it was known only to "members of the [standards] Working Group" that had developed the reference. *Id*., 7.

Petitioner likewise failed to demonstrate that POSITA could find the JEDEC Proposal within the JEDEC online repository (even if they were endeavoring to do so). Petitioner had the burden to describe the "roadmap that would have allowed one skilled in the art" to locate the reference. *SRI*, at 1195-96. Petitioner made no such showing.

Instead, Petitioner relies on the JEDEC representative declaration stating that "[a]nyone interested can join JEDEC online at JEDEC.org," and "any interested

person can join any committee." EX1050, 5. This is inaccurate. JEDEC membership is not (and never was) available to individuals—the JEDEC membership webpage explains that "[m]embership in JEDEC is open to independent entities that manufacture semiconductor products, or provide related services or equipment. Membership is company based, not by individual." EX2014. Petitioner's declaration also omits that JEDEC membership cost $4000/year to join a single committee in 2009, which increased substantially for each additional committee joined. *Id.* And access to JEDEC "committee agendas, minutes, meeting notices and other information that pertains to a specific committee"—e.g., the JEDEC Proposal itself—could be accessed by "members only." EX2013. POSITA would have faced all these barriers to access the JEDEC Proposal, evening assuming they knew it existed. *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1370-73 (Fed. Cir. 2019) ("A work is not publicly accessible if the only people who know how to find it are the ones who created it.").

Petitioner is a member of JEDEC. If POSITA could truly find and access the JEDEC Proposal, Petitioner could surely evidence that. Instead, Petitioner relies on a declaration that documents "such as" the JEDEC Proposal can be accessed by JEDEC *members* on the appropriate committees. Pet., 25-26; EX1050, ¶7. This falls far short of demonstrating that "persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it." *Jazz Pharms.*,

895 F.3d at 1355. Accordingly, the JEDEC Proposal is not "publicly accessible" and not prior art.

VI. Ground 1 Should Be Denied Because the JEDEC Proposal *Postdates* the '218 Patent's June 12, 2009 Priority Date

The Petition argues that the '218 Patent is not entitled to a June 2009 priority date because, according to Petitioner, certain claim elements are not disclosed in the Priority Application. Pet., 4-9. Petitioner is incorrect. EX2001, ¶¶27-46.

A. The Petition Applies the Wrong Legal Standard

The Petition relies on the wrong standard for determining whether the Priority Application adequately discloses claims. There is no "necessarily comprehended" standard, as Petitioner argues (Pet., 5), in determining whether claims are supported by a provisional application's written description. Instead, the provisional application must "clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed," such that "the provisional application "***reasonably conveys*** to those skilled in the art that the inventor has possession of the claimed subject matter as of the filing date." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (emphasis added).

A specification satisfies this requirement when "the essence of the original disclosure" conveys the necessary information—"regardless of how it conveys such information, and regardless of whether the disclosure's words are open to different

interpretations." *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350, 1356 (Fed. Cir. 2015) (alterations omitted). The applicant is ***not*** required "to describe exactly the subject matter claimed" as long as POSITA can "recognize that [the inventor] invented what is claimed.'" *Pandrol USA, LP v. Airboss Ry. Prods.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005); *see Kao Corp. v. Unilever United States, Inc.*, 441 F.3d 963, 968 (Fed. Cir. 2006) ("[T]he disclosure as originally filed does not ... have to provide in *haec verba* support for the claimed subject matter at issue.").

B. The Priority Application Supports the '218 Patent Claims Reciting that "First Edge Connections Are Not Active"

The Petition incorrectly asserts that the claim element requiring "train[ing] with one or more training sequences while the first edge connections are not active," is not sufficiently disclosed in the Priority Application. Pet., 4-7. The Priority Application discloses training sequences during which the "first edge connections are not active"—i.e., when the MCH is not in "normal operation." EX2001, ¶¶27-34.

The Priority Application discloses "[s]haring a pin between the Error-out and Notifying signal," and that a "High" or "Low" signal on that shared pin is used to indicate a different status depending on whether it is being used for an "Error-out" or a "Notifying" signal. EX1008, Fig.3. Specifically, the pin is "[l]ow during MB training" and "a "high signal indicates that training is done." *Id.* Conversely, the

pin is "[h]igh during normal operation unless a parity error occurs." *Id.* A POSITA would therefore understand that it is not technically possible for "MB training" to occur during "normal operation," because the logic on the shared pin conveys different information depending on whether training or normal operation is occurring. EX2001, ¶31. The Priority Application therefore discloses that "normal operation," such as reading and writing to memory, does not occur during training or initialization, and vice versa.

Petitioner itself tacitly concedes this point by going out of its way to argue that training "could occur" or "may (though not necessarily) occur" during "normal operation." Pet., 7-8 ("In fact, as Dr. Alpert explains, a Skilled Artisan would understand training ***could*** occur during normal operation.") (emphasis added). Petitioner's expert previously testified similarly. EX2002, 31:10-32:4 ("I would say it's ***possible*** to do ***certain types*** of training in normal—normal operative mode. … I don't think I can say it ***never*** refers to training, even if you're in normal mode.") (emphases added). This amounts to a concession that the Priority Application, at minimum, would "reasonably convey" to POSITA that training does not occur during normal operation (as was typical), even if it is possible that certain types of training may occur during normal operation. *See Ariad Pharm.*, 598 F.3d at 1351; EX2001, ¶32-33.

The Petition corroborates this. *See* Pet., 6 ("Moreover, it was known before the 2009 provisional filing date that ***some training*** included sending data over the data edge connections, while ***other training did not***.") (emphasis added). Although Petitioner cites no support for this speculation, it is an admission that POSITA would have assumed that training did not typically involve active data pins, even if this was technically possible in some situations. *Id.*; EX2001, ¶33. As discussed above, since the Priority Application discloses different ways of using the "Error-Out pin" during training and normal operations, it is not even technically possible for the normal operation to occur during the type of trainings disclosed in the Priority Application, or vice versa. EX2001, ¶¶30-33. Thus, the Priority Application would "reasonably convey" to POSITA "train[ing] with one or more training sequences while the first edge connections are not active." EX2001, ¶34.

C. The Priority Application Supports the '218 Patent Claims Reciting "One or More Memory Read or Write Operations Not Associated with the One or More Training Sequences"

The Petition incorrectly asserts that the Priority Application does not sufficiently disclose a second mode that is "configured to perform one or more memory read or write operations not associated with the one or more training sequences," as recited in each claim of the '218 patent. Pet., 7-8; EX2001, ¶¶35-40.

Petitioner's only argument on this point is that training ***could*** occur during normal operation, and therefore POSITA would find that training is not "necessarily

excluded" from normal operation. Pet., 7 ("[A] Skilled Artisan would understand training ***could*** occur during normal operation.") (emphasis added). As explained above, this standard is incorrect and irrelevant. The Priority Application plainly discloses "training" that is distinct from "normal operation." EX1008, Fig.3 ("Error-Out pin: Low during MB training … High during normal operation."). The description of Figure 3 makes clear that "MB training" occurs during "initialization." *Id.* 22 ("The output of the notifying signal is low impedance while the memory subsystem controller executing ***each section of the initialization step***, thus the notifying signal is pulled low by the memory subsystem controller."). Indeed, the "low impedance" signal that indicates initialization is juxtaposed in the Priority Application to the "high" signal given during normal operation. *Id.*, 23. This is a ***single*** signal that can only be "low" ***or*** "high," meaning that the "initialization" phase, and therefore the disclosed training (when the signal is "low"), ***cannot occur*** during "normal operation" (when the signal is "high"). EX2001, ¶¶37-38.

The Priority Application explains a change from "training" to "normal operation" may be signaled by a "notifying signal" on the "Error-Out" pin using an "open drain" method. *Id.*, Figs.2-3. Specifically, the "Error-Out pin" is "[l]ow during MB training." *Id*. When training is complete, "a high signal indicates that training is done." *Id.* The signal remains "high during normal operation unless a parity error occurs." *Id.* This unambiguously conveys to POSITA that, when

training is "***done***" (i.e., when the signal is "high"), the module will be in "normal operation" with no ongoing training. EX2001, ¶38.

Furthermore, the Priority Application explains that "training" occurs during "initialization," prior to "normal operation." Specifically, "[t]he output of the notifying signal is low impedance while the memory subsystem controller executing each section of the initialization step, thus the notifying signal is pulled low by the memory subsystem controller." *Id.* The Priority Application therefore "reasonably conveys" to POSITA that, when training is being performed during initialization (i.e., when "the notifying signal is pulled low"), the memory subsystem is not in its "normal operation" and thus is not accessed by the MCH for read or write operations. *Ariad Pharm.*, 598 F.3d at 1351; EX2001, ¶¶36-38.

Petitioner itself essentially concedes this point, going out of its way to argue that training "could occur" or "may (though not necessarily) occur" during "normal operation." Pet., 7-8 ("[A] Skilled Artisan would understand training ***could*** occur during normal operation.")) (emphasis added). Petitioner's expert previously testified similarly. EX2002, 31:10-32:4 ("I would say it's ***possible*** to do ***certain types*** of training in normal—normal operative mode.… I don't think I can say it ***never*** refers to training, even if you're in normal mode.") (emphases added). This concedes that the Priority Application, at minimum, would "reasonably convey" to POSITA that training does not occur during normal operation (as was typical), even

if it is possible that training may occur during normal operation. *Ariad Pharm.*, 598 F.3d at 1351; EX2001, ¶40.

D. The Priority Application Supports the '218 Patent Claims Reciting "One or More" Training "Sequences"

Although the Priority Application discloses performing "MB [Memory Buffer] training," Petitioner incorrectly insists that the Application does not disclose "one or more" training "sequences." Pet., 11. To start, Petitioner's expert has admitted that POSITA would understand that the Priority Application discloses "multiple different types of training." EX2002, 33:17-20. This alone confirms that POSITA would understand that the Priority Application discloses "one or more" training "sequences." EX2001, ¶¶41-46.

Furthermore, the Priority Application also discloses "MB training" and "one or more parts of the initialization operation sequences," which are equivalent (and more lengthy) ways of saying "one or more" training "sequences." EX2001, ¶44. The Priority Application specifically states that "[t]he output of the notifying signal is low impedance while the memory subsystem controller execut[es] ***each section*** of the initialization step." *Id.* at 23. POSITA would therefore understand that the disclosed training occurs during the "initialization operation ***sequences***" (plural) while the "notifying signal is low impedance." EX1008, 22; EX2001, ¶¶44-46. And, as explained above, because the signal can only either be "low" (during

initialization) ***or*** "high" (during normal operation), and because the disclosed "MB training" occurs only when the notifying signal is "low," (EX1008, Fig.3), the training must be performed as during the "initialization operation ***sequences***." EX2001, ¶¶44-46. The Priority Application therefore discloses "one or more" training "sequences" occurring as a part of "initialization operation sequences."

The '218 patent is therefore entitled to the priority date of the Priority Application and, accordingly, JEDEC is not prior art.

VII. Grounds 1-3 Fail Because POSITA Would Not Combine Hazelzet with JEDEC or Buchmann to Arrive at the '218 Patent Claims

Petitioner relies on only two combinations to challenge the independent claims of the '218 patent: (1) Hazelzet with JEDEC ("Ground 1") and (2) Hazelzet with Buchmann ("Ground 2").[1] The Petition contends these combinations are "exceedingly straightforward" (Pet., 32), but they are not. Putting aside that Hazelzet *teaches away* from the alleged combinations, Hazelzet is *incompatible* with the combined references (JEDEC or Buchmann). Indeed, the Petition finally concedes this truth now (Pet., 32)—*after* Petitioner's same expert, addressing the same alleged combinations, admitted during deposition in the prior IPR (IPR2020-

[1] Petitioners' Ground 3—challenging claims 3-6, 10-12, and 17-20 in view of Hazelzet, JEDEC or Buchmann, and Kim (Pet., 4, 67-71)—only challenges dependent claims of the '218 patent. Accordingly, for the same reasons that Petitioner's Grounds 1 and 2 fail, Petitioner's Ground 3 also fails.

01044) that Hazelzet does not have the memory buffer or "the interface that would be—that would be added to Hazelzet in order to be able to perform the—the training sequences that are identified [in JEDEC/Buchmann]." EX2002, 75:10-18; *id.* 78:18-22 ("Hazelzet's buffer would be modified….").[2]

Consequently, *in this Petition*, to make each combination in the Grounds, Petitioner transforms Hazelzet into a Rube Goldberg memory device by first *redesigning* Hazelzet's memory modules and architecture to *add* JEDEC's or Buchmann's memory buffer to buffer the data signals (without demonstrating how—or even if—that could be done); so that Petitioner can then *add* a new "initialization mode ('first mode/operation') into which each [new] module could be switched;" so that Petitioner can then *add* the alleged training sequences of JEDEC/Buchmann to this *new patch-work* memory module, with the new memory module "implement[ing] the training" (because Hazelzet does not disclose training, during initialization or otherwise, and Hazelzet's actual memory modules are incompatible with, and incapable of performing, the JEDEC/Buchmann training); so that, finally, this *new* memory buffer in Hazelzet can report completion of those *new* training

[2] Patent Owner argued the incompatibility of Hazelzet and JEDEC/Buchmann in its §42.120 Response *after* institution of the prior petition (IPR2020-01044, paper 20). However, the Board did not previously consider the Petition's inconsistency because that IPR was terminated shortly after institution. EX1060.

sequences performed in the *new* initialization using a status signal output, *but* using the *pre-transformed* Hazelzet architecture and UE line to do so (but Hazelzet uses a separate bus for initialization—not the UE line). *See* Pet., 32-34; EX2001, ¶¶54-57.

The Petition relies on each step to build upon the previous to transform Hazelzet into something it is not. Accordingly, to show a reasonable likelihood of prevailing on *any* claim of the '218 patent, Petitioner must demonstrate, at minimum, it would have been obvious to make *each and every one* of the above modifications to Hazelzet. The Petition failed on all of these modifications.

A. Summary of Arguments

The Petition paints a false picture that memory modules that buffer data signals (in addition to the address and control signals) were unavailable at the time of Hazelzet, but that once those new memory modules were available, the sequence of Petitioner's multiple transformations of Hazelzet would be obvious, "exceedingly straightforward" and "provid[e] nothing more than expected." Pet., 32-42. As discussed below, this is incorrect and unsupported by the evidence in the Petition.

Memory modules that buffered data signals *and* performed training sequences existed at the time of Hazelzet. EX2001, ¶¶74-75; *see also* EX2004 (US2005/0138267A1), [0023]-[0034], Figs. 4-6 (describing "fully-buffered memory modules" with "built-in self test (BIST)" that "can initiate test sequences."). Yet, tellingly, Hazelzet does not include such memory buffers and does not disclose

training, let alone training *implemented by* the memory buffers. EX2001, ¶¶50, 62. Despite Petitioner's arguments that "advantages of buffering the data lines were well known to a Skilled Artisan at the time" (Pet., 37), and that "it was known that training before normal operation was necessary to minimize errors" (Pet., 39), Petitioner failed to identify a single reference having such memory buffers and training that meet all the limitations of *any* claim of the '218 patent.

Instead, as in the prior IPR (IPR2020-01044), Petitioner relies on the above-referenced combinations of Hazelzet with JEDEC or Buchmann. Also like the prior IPR, Petitioner and its expert assert that "Hazelzet emphasizes the need for '*improved overall system reliability*.'" Pet., 35. And as in the prior IPR, Petitioner and its expert assert that "[g]iven that emphasis, a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training *improved memory module reliability*." Pet., 35-36, 38 ("A Skilled Artisan would have been motivated by these disclosures to look to systems such as JEDEC's and Buchman's *to improve reliability*."); EX1003, ¶151.

But, as discussed above, Petitioner's alleged combinations have a fatal flaw—unrecognized by Petitioner's expert when making these combinations in the prior IPR—in that one *could not* combine the alleged training of JEDEC or Buchmann with Hazelzet because Hazelzet's memory modules are *not compatible* with that training. EX2002, 68:19-79:24, 81:18-83:5; *see also* EX2001, ¶¶54, 63, 67, 85-88.

So here, unlike the prior IPR, Petitioner first argues that "[i]n each [combination], Hazelzet's memory modules would be modified to add the functionality of buffering the data signals similar to that in the DDR3 LRDIMM of the time." Pet., 32; *see* EX2019 (redline of present Petition to IPR2020-01044), 43. Indeed, Petitioner's motivation to add training *now* concedes that JEDEC's and Buchmann's training would have complemented Hazelzet's initialization only "***after*** Hazelzet's DIMM has been updated with a Memory Buffer which buffers both address and data like in JEDEC and Buchmann." Pet., 39; *see* EX2019, 49. But this logic puts the proverbial cart before the horse, and begs the question: why would POSITA have been motivated to change Hazelzet's memory modules as suggested by the Petitioner in the first place?

Petitioner's answer to the question *now*—in view of its otherwise wholesale regurgitation of the prior IPR—exemplifies the hindsight that guided Petitioner and its expert when attempting to recreate the '218 patent claims out of disparate references. Petitioner only argues that POSITA would have been motivated to replace Hazelzet's memory modules to "increase[] performance and capacity." Pet., 37 (citing EX1036, 5); *id.*, 38 (same for Buchmann, "improved performance and higher capacity"). But if "Hazelzet emphasizes the need for '*improved overall system reliability*'"—as Petitioner contends (Pet., 35)—POSITA would *not* be motivated to add more complex memory modules simply to "*increase[]*

performance and capacity." Indeed, Hazelzet expressly teaches away from replacing its memory modules with increased performance and capacity memory modules, focusing instead on "low or midrange server markets" with "simple, relatively inexpensive" "***reduced-function memory assemblies***" that are "cost competitive." EX1014, [0005]-[0006]. Hazelzet even expressly states that a "further object of the present invention is. . . ***eliminating the need to*** produce or ***procure two types of buffer devices*** or to ***re-design existing memory modules***." EX1014, [0014].

Petitioner's alleged motivation to combine Hazelzet's memory modules with the memory buffers of JEDEC or Buchmann so as to then add JEDEC's or Buchmann's training—without demonstrating how such combinations could be done—is pure hindsight, guided solely by the '218 patent disclosure and claims, untethered to what POSITA actually would have been motivated to do in view of the disclosures of Hazelzet and JEDEC or Buchmann. The prior IPR alleged a combination of JEDEC/Buchmann training with Hazelzet. When later exposed that such combination is incompatible, the present Petitioner doubled-down and simply asserted—expressly contrary to Hazelzet's teachings—that it would be "obvious" to replace the memory modules of Hazelzet with a memory module that buffers both address and data "like in JEDEC and Buchmann," for the *sole purpose* of then implementing the training of JEDEC/Buchmann. But, as discussed above, the

Petition's asserted motivation is hollow and Hazelzet teaches away from changing its the memory modules in the first instance. EX2001, ¶¶68-72. Petitioner's arguments can only be the result of hindsight.

Finally, invoking more hindsight analysis, Petitioner then alleges "[i]t would have been further obvious to communicate training status *in an initialization mode* using the same open drain output already used in other modes/operations"—specifically, Hazelzet's UE line. Pet., 40. But there is no teaching or suggestion to do so, and Petitioner provides no articulated reason why POSITA would have been motivated to use Hazelzet's UE line, specifically, as opposed to any other communication line of Hazelzet. Pet., 40-42; EX2001, ¶108. Instead, Petitioner makes a number of generic statements related to POSITA's ability to utilize an open drain output for multiple purposes. Pet., 40-41. But Hazelzet, once again, expressly teaches away from Petitioner's arguments to use the UE line for initialization. EX2001, ¶¶111-114.

Hazelzet specifically discloses "initialization of the memory subsystem" using a bus—not its UE line. EX1014, [0123]-[0125]. Hazelzet teaches that, "[i]n one embodiment, the high-speed bus may be used to complete the initialization of the memory subsystem(s)," e.g., the Error Bus 122. EX1014, [0123], Fig. 4B. Hazelzet also describes that "[a]nother initialization method might utilize ***a distinct bus***, such as a presence detect bus …, an IIC bus … and/or the SMBUS, which has

been ***widely utilized and documented*** in computer systems using such memory modules." EX1014, [0124]. Both examples—the only examples—use a bus, without involving the UE line for initialization.

Hazelzet also expressly addresses Petitioner's argument that POSITA would be motivated to utilize the same pin for multiple uses, teaching that "[t]he use of a ***separate bus*** . . . offers the advantage of providing an independent means for ***both initialization and uses other than initialization***." EX1014, [0125]. Thus, even *if* POSITA added JEDEC/Buchmann training to an initialization mode in Hazelzet (which one wouldn't), Hazelzet teaches away from using the UE line—instead describing the benefits of using a bus during initialization to "connect[] to one or more modules within a memory system …, providing ***an independent means*** of interrogating memory subsystems, programming each of the one or more memory subsystems to operate within the overall system environment, and adjusting the operational characteristics." EX1014, [0124].

Moreover, despite Buchmann also including a UE line, Petitioner's expert previously admitted that Buchmann's UE line does *not* communicate Buchmann's training commands (SBC commands). EX2003, 106:20-107:11; 108:6-14; 124:17-19. Instead, Buchman also sends its training commands via a bus. EX2003, 108:6-14 ("that bus with six lines would carry the SBC [training] command"). None of the cited references describe any benefit or reason to drive a notification signal

associated with the one or more training sequences using an open drain output—Hazelzet does not disclose training and teaches use of a bus during initialization, Buchmann sends its training commands via a bus, and JEDEC does not disclose any benefit or reason to use its ERROUT#. Instead, Petitioner and its expert merely parrot back the benefits of the '218 invention so *as only described in the '218 patent itself*. Pet., 42; EX1003,¶¶168-169.

For these reasons and the reasons below, all Grounds fail at least because the Petition *fails to demonstrate* (1) motivation to *redesign* Hazelzet's memory module to add JEDEC's or Buchmann's memory buffer to buffer the data signals in addition to the address and control signals, and/or how such proposed combinations could be done in Hazelzet's system architecture; (2) motivation to *then add* the kind of alleged training in JEDEC or Buchmann to such redesigned memory module to implement as part of an entirely new type of initialization using JEDEC's or Buchmann's training sequences in addition to Hazelzet's other disclosed operations; and (3) a teaching or suggestion as to how to *then configure* the new patched-up memory module to report completion of the newly inserted training sequences using Hazelzet's *pre-transformed* architecture and UE line.[3] In addition, the proposed

[3] As explained above, Ground 1 also fails because JEDEC (1) is not prior art, and (2) is not a printed publication.

Hazelzet/Buchmann combination, specifically, further fails because there is simply no teaching or suggestion to drive a notification signal associated with the one or more training sequences using an open drain output, which is required by each claim of the '218 patent.

B. The Petition Fails to Demonstrate a Motivation to Redesign Hazelzet's Memory Module to Add JEDEC's or Buchmann's Memory Buffer to Buffer the Data Signals

Both of Petitioner's Grounds require that POSITA would have first, before anything else, redesigned Hazelzet's memory modules to add JEDEC's or Buchmann's memory buffers to buffer data signals in addition to the address and control signals. Specifically, Petitioner argues, "[i]n each [combination], Hazelzet's memory modules *would be modified to add* the functionality of buffering the data signals similar to that in the DDR3 LRDIMM of the time." Pet., 32. Each combination is predicated on Petitioner's contention that "[a]lthough Hazelzet discloses a Registered DIMM (RDIMM), it would have been obvious to update Hazelzet's RDIMM to a LR-DIMM of JEDEC." Pet., 36, *see id*., 39 ("***after*** Hazelzet's DIMM has been updated with a Memory Buffer which buffers both address and data like in JEDEC and Buchmann."). All Grounds require this modification to Hazelzet in order to succeed because, as discussed above, Hazelzet's disclosed memory modules are incompatible with JEDEC's and Buchmann's

alleged training in an initialization mode (Petitioner's second modification to Hazelzet). EX2002, 68:19-79:24, 81:18-83:5; *see* EX2001, ¶¶59-63.

Despite contending that POSITA would have fundamentally changed the memory architecture of Hazelzet, Petitioner provides only a short, conclusory reason for doing so, namely "increased performance and capacity":

> The LRDIMM Design Specification explained in detail the advantages, including *increased performance and capacity*, of adding the LRDIMM's data buffering functionality to an RDIMM, like Hazelzet's module, which buffers only address and command signals. EX1036, 5. Thus, a Skilled Artisan would have understood and been motivated at the time to upgrade Hazelzet's RDIMM with an LRDIMM functionality to buffer the data lines as well.

Pet., 37.[4] Petitioner provided the same conclusory opinion in view of Buchmann. *See* Pet., 38 ("improved performance and higher capacity, as discussed above"). Petitioner offers no other reason to change the memory module of Hazelzet, and simply states that "[s]uch an upgraded LRDIMM would have worked even in Hazelzet's RDIMM platforms (with appropriate BIOS changes)." Pet., 37. But just

[4] Petitioner contends that "LRDIMM Design Specification explained in detail the advantages." However, the full disclosure is simply: "The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load." EX1036, 5. This is not a "detailed explanation" and does not describe any additional advantage other than increased performance and capacity.

because one *could* increase performance and capacity, it does not follow that one *would* be motivated to do so. *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed.Appx. 1019, 1027 (Fed. Cir. 2016) ("what one of skill in the art . . . 'could have' done to meet the limitation . . . is not sufficient").

Because the prior IPR (IPR2020-01044) did not allege that POSITA would redesign Hazelzet's memory modules, and because Patent Owner did not argue the resulting incompatibility of Hazelzet and JEDEC/Buchmann until its §42.120 Response *after* institution (IPR2020-01044, paper XX), the Board did not previously consider the foundational premise of whether it would have been obvious to first redesign Hazelzet's memory modules. As discussed below, Hazelzet teaches away from adding more complex data line buffers to its memory architecture. Therefore, POSITA would not have been motivated to add a buffer to the data path of Hazelzet's disclosed memory modules. Petitioner's failure to demonstrate that POSITA would have modified Hazelzet's disclosed memory modules in the first instance is an independent reason that all Grounds fail.

1. Hazelzet Teaches Away from "Upgrading" Its Memory Modules to Buffer the Data Signals

Petitioner's motivation argument is akin to being motivated to "upgrade" a Fiat to a Ferrari simply because a Ferrari has increased performance. But like a Fiat, Hazelzet does not emphasize performance and capacity; instead, Petitioner contends

"Hazelzet emphasizes the need for 'improved overall system reliability.'" Pet., 35. Yet, Hazelzet did not focus myopically on the system's reliability to the detriment of its performance, capacity or cost. Instead, Hazelzet considered all of these factors and sought a solution that would strike a balance between performance, capacity, reliability, and cost for low or midrange systems. EX1014, [0001]-[0006]; EX2001, ¶¶69-70. Hazelzet's ultimate solution/disclosure teaches away from replacing its memory modules with increased performance and capacity memory modules, focusing instead on improving the system reliability in memory modules for "low or midrange server markets" that used "simple, relatively inexpensive" "***reduced-function memory assemblies***" having an "adequate level of asset-protection" at "low cost." EX1014, [0005]-[0007]. Moreover, Hazelzet teaches "***eliminating the need to*** produce or ***procure two types of buffer devices*** or to ***re-design existing memory modules***." EX1014, [0014]; EX2001, ¶71.

Reading Hazelzet, POSITA "would be led in a direction divergent from" adding more complex memory components that buffer data signals in addition to buffering the address and control signals, which itself would be opposite of Hazelzet's intended purpose to use "reduced-function memory assemblies" for the "low or midrange server markets." *See In re Gurley*, 27 F.2d 551, 553 (Fed. Cir. 1994); EX2001, ¶¶68-72, 76. Petitioner's conclusory motivation driven only by increased performance and capacity failed to consider Hazelzet's disclosure as a

whole, which considered a balance of trade-offs between reliability, performance, capacity and cost. One cannot "stitch together an obviousness finding from discrete portions of prior art references without considering the references as a whole." *In re Enhanced Security Research, LLC*, 739 F.3d 1347, 1355 (Fed. Cir. 2014).

2. Petitioner's Motivation to "Upgrade" Hazelzet's Memory Module is Conclusory

Petitioner's alleged "increased performance and capacity" motivation is conclusory. As discussed above, Hazelzet considered a number of factors, including reliability, performance, capacity and cost when designing that memory system. Despite a number of different ways POSITA may increase memory performance and capacity, Petitioner states that adding "a Memory Buffer which buffers both address and data like in JEDEC and Buchmann," alone, would be the only obvious choice. Pet., 37-39; EX1003, ¶154-156.

Petition failed to address that memory modules that buffered data signals (in addition to the address and control signals) *and* performed training sequences already existed at the time of Hazelzet. EX2001, ¶¶74-75; *see also* EX2004 (US2005/0138267A1), [0023]-[0034], Figs. 4-6 (describing "fully-buffered memory modules" that buffer data, address and control signals, and implement "built-in self test (BIST)" function that "can initiate test sequences to test the device's memory channels and/or test the DRAM devices."); EX2015, [0014]-[0016], [0023] [0039],

[0048]-[0052]; EX2016, 4, 5, 24, 30.[5] Yet Hazelzet itself did not include such memory for its "reduced-function memory assemblies." Moreover, even years after the introduction of LRDIMMs, the industry still debated the trade-offs of LRDIMMs and RDIMMs, recognizing that different overall system configurations and requirements counsel use of one or the other. EX2001, ¶76; e.g., EX2006, 1 ("We have encountered many clients that assume since the LRDIMM is the newest memory on the block, it must be the best memory to use in their newest server. However, this is often not the case!"); EX2017, 1 ("The critical factors to consider are latency, speed, and capacity, along with what your computing objectives are with respect to them."). The Petition failed to demonstrate POSITA would have been motivated to redesign Hazelzet's memory architecture to incorporate JEDEC's or Buchmann's memory buffers.

Nor does the Petition demonstrate how the proposed combination could have been done (or that there would have been a reasonable expectation of success in doing so). Petitioner merely makes the conclusory contention that "[s]uch an upgraded LRDIMM would have worked even in Hazelzet's RDIMM platforms (with

[5] US2005/0138267A1 was submitted to the PTO by the applicants of Hazelzet during prosecution of the Hazelzet application. EX2005 (US7,870,459, References Cited).

(Cont'd on next page)

appropriate BIOS changes)." Pet., 37 (citing EX1036). Instead of providing any support for this conclusory contention,[6] the same document cited by Petitioner contradicts the assertion, stating that "[a]s defined the controller must have the capability to do address mirroring." EX1036, 5. Hazelzet does not have a controller with the capability to do address mirroring (EX2001, ¶79); Petitioner does not allege that it does. Nor does Petitioner or its expert address the contemporaneous art detailing the problems associated with LRDIMMs or address how POSITA would implement LRDIMMs in Hazelzet. *See* EX2001, ¶¶80-83; *see also* EX2007 (US 8,402,208), 1:37-61 (LRDIMMs complicate memory configuration); EX2008 (US 8,452,917), 2:12-30 (LRDIMMs cause mismatched signals between host and memory interface); EX2009 (US Pub. 2011/0007585), [0003] (reduced timing margins); EX2010 (US 8,054,664), 4:8-61 (describing a number of problems implementing LRDIMMs). Moreover, despite Petitioner's reliance on its expert's opinion that the "combination would have been well within the level of skill at the time" (Pet., 37; EX1003, ¶156), when making the same combination, Petitioner's expert previously testified that his analysis was "not concerned with the physical

[6] Petitioner's expert merely parrots back the same conclusory assertion that a "Skilled Artisan would have been further motivated to make such an upgrade because the LRDIMM would have worked even in RDIMM platforms (with appropriate BIOS changes), thus it was possible to achievethese advantages in existing, RDIMM based systems, like in Hazelzet." EX1003, ¶155.

embodiments and how… those structures might be physically modified. … I haven't considered what—you know, exactly how those changes would be made." EX2002, 68:19-69:20.

The conclusory testimony of Petitioners' expert does not provide an articulated motivation to change Hazelzet's memory modules by adding JEDEC's or Buchmann's memory buffers, or demonstrate that such combination could even be done. Conclusory statements do not amount to substantial evidence. *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019).

3. Petitioner's Motivation to "Upgrade" Hazelzet's Memory Module Is the Result of Hindsight

The history of Petitioner's expert's opinions also demonstrate hindsight. Petitioner's expert declaration from Dr. Alpert in the present IPR is substantially the same as his declaration in the prior IPR (EX2020, Exhibit 1003 to IPR2020-01044 Petition)—save for Dr. Alpert's new opinion, foundational to the present Petition, that POSITA would first modify Hazelzet's memory module to buffer the data lines like JEDEC or Buchmann. As explained above, the reason for now including this opinion is self-evident; Petitioner needs to add yet another missing link to its hindsight reconstruction of the '218 patent claims.

In the prior IPR, Dr. Alpert opined that POSITA would have been "motivated to combine Hazelzet and JEDEC or Buchmann in a training mode occurring before,

and separate from, other, normal operating modes" because they "would have complemented that power-up process as part of Hazelzet's initialization." EX2020 (Exhibit 1003 to IPR2020-01044), ¶143; *see also* EX2019 (redline of present Petition to IPR2020-01044), 49. Dr. Alpert did not, however, previously opine that POSITA would have been motivated to first modify the Hazelzet memory modules as he does in the present Petition. During his deposition in that prior IPR, the fatal flaw in his prior opinion was exposed in that one *could not* combine the alleged training of JEDEC or Buchmann with Hazelzet because Hazelzet's memory module and buffer *could not* implement that training. EX2002, 68:19-79:24, 81:18-83:5. *See In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed.Cir. 2007) ("[A] reference teaches away from a combination when using it in that combination would produce an inoperative result.").

Thus, here, Dr. Alpert has amended his opinion regarding the same combinations of art, now stating that POSITA would *first* be motivated to change Hazelzet's memory modules to increase performance and capacity. With a slight of hand, Dr. Albert now opines that *because* POSITA would have *first* "upgraded" Hazelzet's memory by adding JEDEC's or Buchmann's memory buffers, it would *then* follow that POSITA "would have been *also motivated* to use the initialization techniques of" the "upgraded" memory modules. EX1003, ¶156; Pet., 37. Indeed, in contrast to the prior IPR, Petitioner here concedes that JEDEC's/Buchmann's

training would have complemented Hazelzet's initialization only "***after*** Hazelzet's DIMM has been updated with a Memory Buffer which buffers both address and data like in JEDEC and Buchmann." Pet., 39; *see* EX2019 (redline of present Petition to IPR2020-01044), 49.

Petitioner, and Dr. Alpert, have thus changed the argument. No longer would JEDEC/Buchmann's training simply "compliment" Hazelzet's initialization, as argued in the prior IPR (because they are incompatible), but instead, Petitioner now argues JEDEC/Buchmann would "compliment" Hazelzet only *after* it is materially modified. Petitioner's and Dr. Alpert's motivation to *first* change Hazelzet's memory modules, in order for JEDEC's/Buchmann's training to *then* compliment it, is backwards looking hindsight. *See*, *e.g.*, *ATD Corp. v. Lydall , Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) ("Determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.").

C. There Is No Motivation to Create a Separate Training Mode in Hazelzet, Let Alone the Specific Training of JEDEC/Buchmann

Both of Petitioners' Grounds further require—after first redesigning Hazelzet's memory modules by adding JEDEC's or Buchmann's memory buffers—to then add the alleged training of JEDEC or Buchman during Hazelzet's initialization. Pet., 4, 32-33, 35-40. To demonstrate it would have been obvious to

add JEDEC/Buchmann training specifically, Petitioner must first demonstrate it obvious to add *any* training.

As an initial matter, as discussed above, it would not have been obvious to implement JEDEC/Buchmann training in Hazelzet because such a combination is inoperable by Hazelzet's memory module. *See In re ICON*, 496 F.3d at 1382. Petitioner's alleged motivation to first modify Hazelzet's memory module—for the sole purpose of facilitating Petitioner's implementation of JEDEC/Buchmann training in that *modified* Hazelzet configuration—is illogical, conclusory, and born of hindsight.

Setting aside Petitioner's hindsight analysis just to position itself to the point where such a combination *might* be operable in a modified Hazelzet, Petitioner concedes that "the circuitry of Hazelzet's module, in particular the ECC/Parity register, would [also] *be modified* to implement the training as part of an additional mode to run." Pet., 33. But once again, Petitioner provides no evidence or explanation as to why the addition of an entirely new mode of operation would have been obvious and "straightforward." (Pet., 35-39). Quite the opposite is true. Adding an entirely new mode of operation would require substantial reconstruction and redesign of Hazelzet. EX2001, ¶¶85-88. Petitioner's expert conceded this point during deposition in the prior IPR, admitting that adding a new mode of operation to a memory module like Hazelzet would include fundamental and complex

redesigns to the entire system, which would then have to be tested "extensively." EX2002, 70:3-76:10. Despite previously acknowledging these very issues, Petitioner and its expert still failed to address any of them when discussing how POSITA would allegedly add a new training mode to Hazelzet. Pet., 32-40.

Accordingly, Petitioner failed to demonstrate that redesigning Hazelzet's ECC/Parity register to accommodate *any* training in a new initialization mode would have been obvious—which is a predicate hurdle before even considering whether it would have been obvious to implement *the specific training* of JEDEC/Buchmann (as opposed to any other known training). *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (holding the suggested combination of references improper under §103 because it "would require a substantial reconstruction and redesign of the elements shown in [a prior art reference] as well as a change in the basic principles under which [that reference's] construction was designed to operate").

Petitioner also failed to demonstrate there would be a reasonable likelihood of success in modifying Hazelzet as asserted. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Petitioner's failure to substantiate its bald assertion that it "would have been well within the level of skill at the time" for POSITA to simply *further modify* Hazelzet's ECC/Parity register to implement the alleged training in combination (Pet., 37-38) is a separate, independent reason why the Petition failed to demonstrate POSITA would have been motivated, or even understood how, to

add training in Hazelzet as a new initialization mode—whether JEDEC/Buchmann training or otherwise.

As discussed below, not only is Petitioner's contention that POSITA would have modified Hazelzet to add training in an initialization mode insufficient to institute, so too is Petitioner's further argument that POSITA would have *specifically added* JEDEC's or Buchmann's training in that new training mode.

1. Hazelzet, JEDEC and Buchmann Teach *Different* Solutions to *Different* Problems

Petitioner alleges that "Hazelzet emphasizes the need for 'improved overall system reliability,'" and thus, POSITA "would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability." Pet., 35-36. Although Petitioner characterizes both training (JEDEC/Buchmann) and error code correction (ECC) (Hazelzet) as generically related to "reliability," training and ECC are fundamentally *different* solutions to *different* problems in memory modules.

Training seeks to pre-emptively correct timing issues, particularly in memory systems that deploy buffering on the data lines—like those in Buchmann's high-speed link or JEDEC's LRDIMMs—because in those systems the memory devices are hidden from the memory bus behind a buffer. EX1015, 8; EX1016, 1:1-2:61, Figs. 1&2; EX2001, ¶¶96-98. From the perspective of the memory controller,

each component on a memory module is a slightly different distance away, and each component takes a slightly different amount of time to perform an operation. EX1015, 8; EX1016, 3:49-4:28, 5:13-65, 7:14-24, 8:14-29, 9:18-24, 10:5-65, 12:7-59, Figs. 1&13; EX2001, ¶98; EX2011, 195. Memory modules without training typically included a predetermined constant for timing that balance these concerns by erring on the side of allowing more time. EX2001, ¶98. Training reduces the amount of time by synchronizing the data transfer to a clock signal. EX2014, 3:61-4:28, 4:51-6:50, Fig. 3; EX2001, ¶96; EX2011, 195. The trade-offs are system costs and complexity to implement training with the efficiency to be gained. EX2001, ¶¶96-98.

ECC, on the other hand, cannot and does not seek to optimize the timing of signals between memory controller and memory module components. EX2001, ¶¶93-95, 99. ECC is used to correct errors in data packets that are *already sent* by including redundant information in each data packet. EX1014, [0008], [0016]-[0022], [0035]-[0044], [0059], [0063]-[0069]; EX2012, 764-766. Upon receipt of the data packets, an algorithm compares all the data to determine whether there are any errors, and if so, uses the redundant information to correct those errors. *Id.*; EX2001, ¶99. Thus, ECC corrects data errors once they have occurred, and, in contrast, Buchmann's and JEDEC's alleged training is used to prevent timing errors from occurring before they do. EX2001, ¶¶93-100.

Shipping a package is a useful analogy to highlight the differences between ECC and training. EX2001, ¶100. Training is used to determine when a package should be sent to ensure that the intended recipient is available for delivery. If the package is sent too early or too late, the intended recipient will not be home to receive it. Training makes sure that the shipping company sends the package at a time when the recipient is home. ECC, on the other hand, seeks to ensure that the right content is sent in the package, and, if not, resend the correct content. This is done without regard for when the package is sent. For example, ECC ensures that if a basketball is intended to be shipped, a basketball is ultimately shipped. If, instead, a football is shipped, ECC will correct that mistake by resending a package that includes a basketball. Thus, training (as in JEDEC and Buchmann) and ECC (taught by Hazelzet) are fundamentally different solutions to different reliability problems.

Hazelzet's alleged emphasis (Petitioner's alleged motivation) for "improved overall system reliability" is unrelated to training. Hazelzet considered a balance of trade-offs between reliability, performance, capacity and cost for low or midrange systems ("reduced function memory assemblies") having an "adequate level of asset-protection." EX1014, [0001]-[0014]. With these considerations in mind, Hazelzet teaches the use of parity to enhance its system's performance and ECC to enhance reliability. EX2003 (Alpert Deposition), 65:13-19. Despite Petitioner's

argument that "it was known that training improved memory module reliability" (Pet., 36), and that "Hazelzet emphasizes the need for 'improved overall system reliability'" (Pet., 35), Hazelzet makes no mention of training—even in its contemplated alternative solutions to increase reliability in low-end memory systems. EX1014, [0005], [0127], [0128]; EX2001, ¶¶90-91. Indeed, Petitioner's expert emphatically stated that Hazelzet does not have training. EX2002, 52:17-22; 53:13-18. Notwithstanding, Petitioner alleges that POSITA would have been motivated to add training, and specifically the alleged training disclosed in Buchmann and JEDEC, to Hazelzet during initialization. Pet., 35-40.

But Petitioner failed to demonstrate *why* POSITA would be motivated to specifically add JEDEC/Buchmann training to Hazelzet in order to "improve overall system reliability"—to the exclusion of the myriad of other techniques, many of which are already implemented or identified in Hazelzet (EX1014, [0005], [0127] and [0128]). EX2001, ¶¶90, 104-105. Hazelzet presents a different memory module from that of Buchmann or JEDEC, and solves "reliability" in that system using ECC. Timing uncertainty (for which training is one solution) is a *different* problem than Hazelzet attempted to resolve. Indeed, Hazelzet does not deploy data buffering on the data lines, and thus, did not need to (and POSITA would not have been motivated to) address this type of problem in Hazelzet's memory system with training. Thus, POSITA would not be motivated to also add training—there is no teaching or

suggestion of any other problems in Hazelzet's system to be solved using training besides the alleged motivation of "improved overall system reliability," which Hazelzet already resolved with ECC. EX2001, ¶103; *see Arris Int'l PLC v. Sony Corp.*, IPR2016-00828, Paper 10 at 15-16 (PTAB Oct. 7, 2016) (denying institution and rejecting petitioner's obviousness rationale that "fails to acknowledge that [the primary prior art reference] already provides a different solution to the problem identified by Petitioner"); *see also Front Row Techs. v. MLB Advanced Media, L.P.*, IPR2015-01932, Paper 7 at 17 (PTAB Mar. 25, 2016) (denying institution and rejecting petitioner's basis for combining the prior art "to utilize a ticket selling device in place of a ticket seller" as "not persuasive reasoning or even a motivation to combine" since the primary prior art reference "already utilizes various ticket selling devices").

Indeed, the mere "recognition of a need does not render obvious the achievement that meets that need. There is an important distinction between the general motivation to cure an uncured disease…, and the motivation to create a particular cure... Recognition of an unsolved problem does not render the solution obvious." *Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc.*, 381 F.3d 1371 (Fed. Cir. 2004). Here, like *Cardiac Pacemakers*, Petitioners offer a cure (training) to an alleged problem (increased reliability) that has already been resolved (Hazelzet's ECC). But even more egregious, Petitioner offers a cure (training) to a *specific*

reliability problem (timing) that doesn't even exist in Hazelzet—at least not until *Petitioner* itself *modified* Hazelzet to include buffering of the data lines that thereby introduces the problem JEDEC's and Buchmann's training are intended to solve. Indeed, Petitioner's motivation is backwards—Petitioner offers a cure to a problem that Petitioner introduces, not one that existed in Hazelzet to start. This does not demonstrate obviousness or a motivation to add training to Hazelzet, let alone the specific type of training alleged to be disclosed in Buchmann or JEDEC. EX2001, ¶103.

Upon reading Hazelzet, POSITA would be discouraged from following the path set out in the '218 patent (or JEDEC or Buchmann), and instead, would be led in a direction divergent from modifying its memory modules and adding training. *In re Gurley*, 27 F.2d at 553; *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326 (Fed. Cir. 2009). Unlike JEDEC and Buchmann, which chose training of their particular memory modules (which are fundamentally different than Hazelzet's memory modules) during initialization as a method to improve overall system reliability, Hazelzet teaches ECC to improve reliability after contemplating numerous other techniques—none of which involved training during initialization. Accordingly, Hazelzet's teaching would lead POSITA on a path that diverges from the one taken by the '218 patent. EX2001, ¶107.

2. Petitioners' Motivation to Combine Is Again the Result of Hindsight

Petitioner's explanation why POSITA would have been motivated to add JEDEC's/Buchmann's training to Hazelzet is circular and illogical. At bottom, Petitioner first argues that POSITA "would have been motivated to add training to Hazelzet because it was known that training improved memory module *reliability*." Pet., 36. But Hazelzet's memory modules are incompatible with JEDEC/Buchmann training. *Supra* Section VII.B. So Petitioner then argues POSITA would have been motivated to replace Hazelzet's memory module with that of either JEDEC or Buchmann because it would "increase[] *performance and capacity*." Pet., 37-38. And only then, having now changed Hazelzet's buffer configuration with JEDEC's or Buchmann's buffer configuration, argues POSITA "would have been also motivated to use the initialization techniques of [the JEDEC/Buchmann memory modules]." Pet., 37 (JEDEC), 38 (Buchmann). Such a circular argument fails to demonstrate a motivation to combine the references. "[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418-19. Instead, "a range of real-world facts to determine 'whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue'"

must be considered. *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1344 (Fed. Cir. 2017).

POSITA would not have been motivated to first change Hazelzet's memory modules, to then modify Hazelzet's ECC/Parity register, and only then add JEDEC/Buchmann training as part of a new mode run during initialization. Neither Petitioner, nor its expert, provide a coherent motivation for POSITA to jump through all these hoops just to add Buchmann's or JEDEC's alleged training to Hazelzet. EX1003, ¶¶161-163. Petitioner's reliance on the conclusory testimony of its expert does not amount to substantial evidence. *TQ Delta*, 942 F.3d at 1358.

D. There is No Teaching, Suggestion or Motivation to Use Hazelzet's UE Line to Communicate Training Signals

Completely separate from Petitioner's failure to demonstrate POSITA would first change Hazelzet's memory modules and then implement JEDEC's or Buchmann's training in Hazelzet during initialization (discussed above), the Petition also failed to demonstrate POSITA would have been motivated to arrange the "*modified* Hazelzet" to communicate signals associated with training in the ways claimed in the '218 patent. Pet., 40-42.

Both Grounds require that POSITA would configure Hazelzet's *new* memory module to report completion of the *new* training sequences performed in the *new* initialization mode using Hazelzet's *pre-transformed* architecture and UE line. Pet.,

33-34, 40-42. Petitioner alleges "[i]t would have been further obvious to communicate training status *in an initialization mode* using the same open drain output already used in other modes/operations"—specifically Hazelzet's UE line. Pet., 40-42. But there is no teaching or suggestion to do so, and Petitioner provides no articulate reason why POSITA would have been motivated to use Hazelzet's open drain UE line, *specifically*, as opposed to any other communication line of Hazelzet. Pet., 40-42; EX2001, ¶108. Instead, Petitioners makes a number of generic statements related to POSITA's ability to utilize an open drain output for multiple purposes. Pet., 40-41. The Petition completely ignores, however, that Hazelzet expressly teaches away from using its UE line during initialization—teaching instead to use a bus.

Petitioner's reliance on Buchmann and JEDEC do not "fill the gap." Buchmann, although having a UE line, does *not* use its UE line to communicate training signals. Instead, like Hazelzet's initialization, Buchmann also uses a separate bus. JEDEC does not have a UE line; but, JEDEC does have an SMBus (EX1015, 8), which Hazelzet teaches to use during its initialization (JEDEC's training is performed during initialization (Pet., 29)).

Without a clean tie between the references that would teach or suggest POSITA to use Hazelzet's UE line, specifically, to communicate signals associated with Petitioner's new theoretical training in Petitioner's new theoretical initialization

mode—and with none of the cited references describing *any benefit or reason* to communicate training status using an open drain output—Petitioner relies on its expert to "fill the gap" by citing generic passages in Hazelzet (which, as discussed below, expressly teaches away), Kim (EX1017) and James (EX1043) that *do not* disclose the novel arrangement claimed in the '218 patent. Pet., 42; EX2001, ¶109. Petitioner's expert then attempts to transform these generic statements into the arrangement claimed in the '218 patent by simply parroting back the benefits for doing so *as only described in the '218 patent*. Pet., 42; EX1003,¶¶168-169.

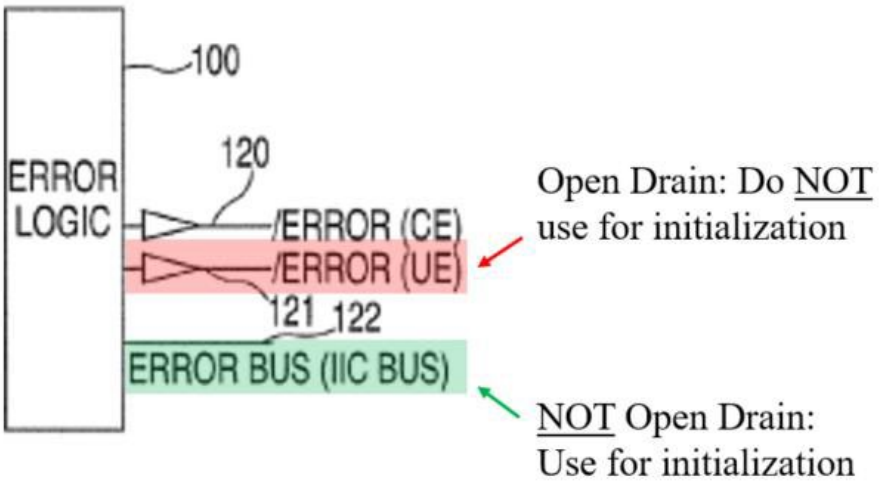
1. Hazelzet Teaches Away from Using its UE Output During Initialization

As an initial matter, Petitioner argues that because "Hazelzet uses the same open drain output, UE 121, to indicate an 'uncorrectable error' in ECC mode and parity error in parity mode," it would have been obvious "to use that same output in the *added* training mode/operation" since "those modes would not be using the open drain outputs while the training operation was running during initialization." Pet., 40-41. This argument is facially deficient for multiple reasons.

First, training status is not an "error" and thus not an analogous signal to Hazelzet's UE line signals. Second, Petitioner ignores, and doesn't even consider, that there would be a number of other unused pins available while Petitioner's theoretical Hazelzet/JEDEC or Hazelzet/Buchmann training operation was running

during initialization. EX2001, ¶108. Hazelzet has a total of 276 pins "for electrically connecting the external circuitry to the SDRAMs in a direct or indirect manner." EX1014, [0015], Figs. 7A-7C. That Hazelzet's UE line is used in both ECC and parity is not itself a motivation, teaching or suggestion to use that specific output in a new "*added* training mode/operation." Just because POSITA *could* use the UE line, does not mean POSITA *would* have been motivated to use it. *Black & Decker*, 646 Fed.Appx. at 1027. Indeed, POSITA would not have been motivated to use Hazelzet's UE line for any training signals.

Fatal to the Petition's alleged combinations, Hazelzet expressly teaches away from using its UE pin during initialization. Instead, Hazelzet consistently—and only—discloses "initialization of the memory subsystem" using a bus, which is distinct from its UE line. EX1014, [0123]-[0125]. Specifically, Hazelzet teaches that "[i]n one embodiment, the high-speed bus may be used to complete the initialization of the memory subsystem(s)," e.g., the Error Bus 122. EX1014, [0123], Fig. 4B; EX2001, ¶111. Hazelzet also describes that "[a]nother initialization method might utilize ***a distinct bus***, such as a presence detect bus …, an IIC bus … and/or the SMBUS, which has been ***widely utilized and documented*** in computer systems using such memory modules." EX1014, [0124]. Both examples—the only examples of initialization in Hazelzet—use a bus, without involving the UE line for initialization.



See EX1014, Figure 4B (annotated); EX2001, ¶111.

Moreover, Hazelzet also directly addresses Petitioner's argument that POSITA would be motivated to utilize the same pin for multiple uses, expressly teaching the benefits of using a bus:

> The use of a separate bus… also offers the advantage of providing an independent means ***for both initialization and uses other than initialization***, such as described in U.S. Pat. No. 6,381,685 to Dell et al., of common assignment herewith, including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.

EX1014, [0125]. Thus, even *if* POSITA added JEDEC's or Buchmann's training to an initialization mode in Hazelzet (which POSITA wouldn't), Hazelzet teaches away from using the UE line and to instead use a bus for initialization to "connect[] to one or more modules within a memory system" thereby "providing ***an independent means*** of interrogating memory subsystems, programming each of the one or more

memory subsystems to operate within the overall system environment, and adjusting the operational characteristics at other times during the normal system operation based on performance, thermal, configuration or other changes desired or detected in the system environment." EX1014, [0124]. Accordingly, Hazelzet not only teaches use of a bus during initialization, but it also describes the advantages of doing so, thereby expressly teaching away from using its UE pin.

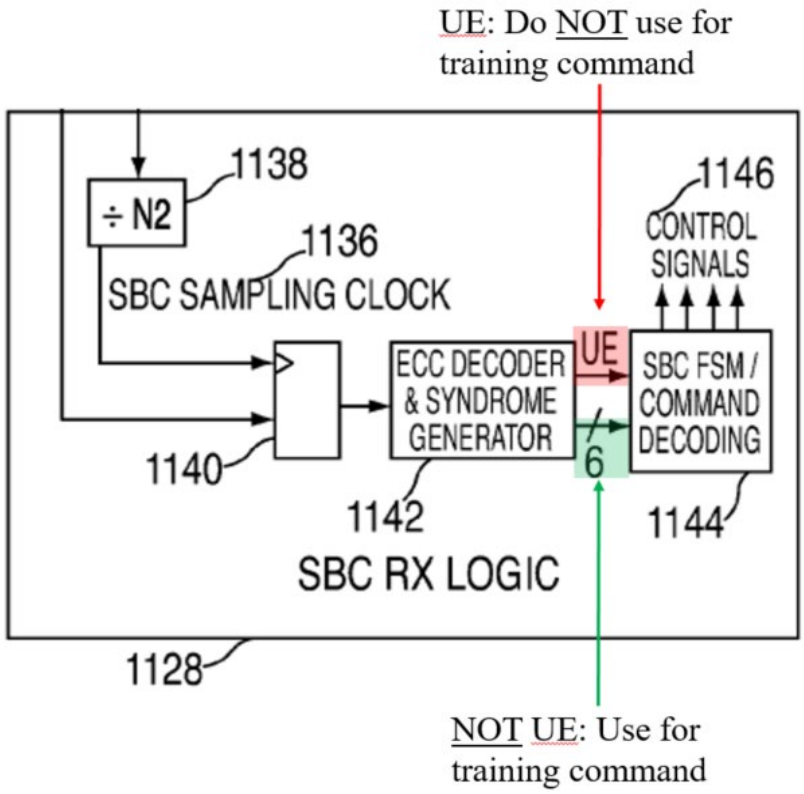
Thus, POSITA would not be motivated to use Hazelzet's UE line to communicate as Petitioner suggests in conclusory fashion; instead, as expressly described by Hazelzet, POSITA would be motivated to reuse Hazelzet's IIC bus (or use another distinct bus such as an SMBus) for initialization. EX2001, ¶¶112-114.

2. The Claims of the '218 Patent Are Not Obvious Over Hazelzet In View of Buchmann Because Neither Teach or Suggest Using Any Open Drain Output for Signaling During Initialization

Incredibly, but not surprisingly, Buchmann also expressly discloses communicating training signals over a bus—not its UE line or an open drain output.

Petitioner alleges that Buchmann's TS/SBC commands (specifically, TS0_done, TS3_ack, and TS3_done) would be obvious to output via Hazelzet's UE line in order to satisfy the claimed "associated with the one or more training sequences" and "wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences." Pet., 32-33,

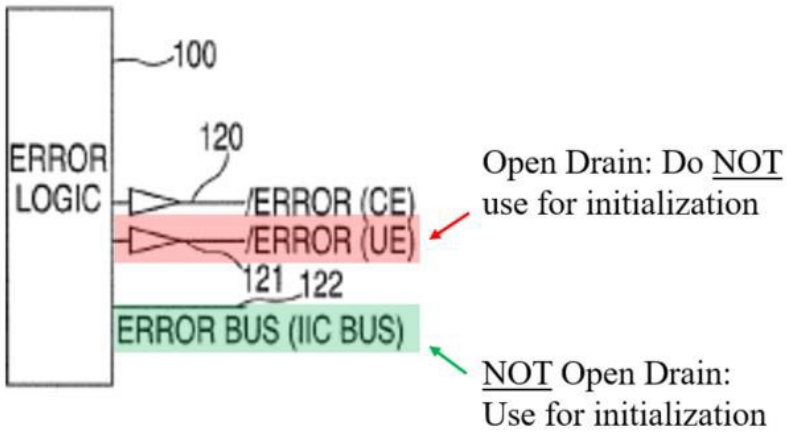
54-55. However, although Buchmann includes a UE line, Petitioner's expert previously admitted that Buchmann's UE line does *not* communicate Buchmann's training commands (TS/SBC commands). EX2003, 106:20-107:11; 108:6-14; 124:17-19. Instead, Petitioner's expert confirmed that Buchman also sends its training commands (TS/SBC commands) via a bus. EX2003, 108:6-14 ("that bus with six lines would carry the SBC command" [referring to Buchmann, Figure 11 (below)]); Pet., 30 (Buchmann "discloses executing training sequences in SBC mode"). Buchmann's UE line (annotated red), which does *not* send training commands, and the separate bus (annotated green), which *does* communicate training commands, are depicted in Figure 11 of Buchmann below:



EX1016, Fig. 11 (annotated); EX2001, ¶116.

As Petitioner's expert also explained, Buchmann's training signals are output via a bus—and not over the UE line—for good reason. Buchmann's SBC training commands are six-bits, and thus, the "bus with six lines would carry the SBC command." EX2003, 102:2-4; 108:6-14; *see also* EX1016, 18:66-19:14, Table 11. On the other hand, the UE line is only a one-bit signal. EX2003, 108:15-109:2. Thus, as previously confirmed by Petitioner's expert, Buchmann's UE line does not output Buchmann's training commands. EX2001, ¶117.

As discussed above (Section VII.D.1), like Buchmann, Hazelzet also teaches use of a bus—not the UE line—for initialization.



EX1014, Fig. 4B (annotated); EX2001, ¶118. Accordingly, both Buchmann and Hazelzet disclose teachings that diverge from the '218 claims. The modification and combination proposed by the Petition do not make the '218 claims obvious; instead,

they teach away from the '218 claims. *In re Gurley*, 27 F.2d at 553; *DePuy Spine*, 567 F.3d at 1314.

In addition, despite relying on Buchmann's TS3 commands, Petitioners' expert previously conceded that Buchmann's TS3 commands "wouldn't necessarily be a very appropriate command" for Hazelzet. EX2003, 121:6-15. Neither Petitioner, nor its same expert here, makes any attempt to explain why TS3 commands would be a good fit for Hazelzet now, and makes no attempt to explain why Buchmann's TS0 commands—or any other TS command for that matter—are appropriate commands for inclusion in Hazelzet. In fact, Petitioners' expert did not even know the significance of Buchmann's particular TS3 commands when previously making the same combination of Hazelzet and Buchman. EX2003, 103:3-11. Illustrative of the Petition's hindsight analysis in this regard, Petitioners' expert previously testified that there are many ways Buchmann's six-bit message could be implemented in Hazelzet, and his only rationale for adding it to Hazelzet's UE line was that he "d[id]n't see a reason why the UE line couldn't be used for that purpose." EX2003, 126:15-24. And even then, Dr. Alpert admitted that to do so, one would also have *further change* Buchmann to communicate the six-bit training signals serially, as opposed to in parallel as actually described in Buchmann. *Compare id.*, *with* 104:511 ("I don't believe this would be showing a serial path for transmitting the 6 bits of commands."). Petitioner's and its expert's contentions

amount to conclusory, unsupported, prognostication directly contradicted by the disclosures in both Hazelzet and Buchmann. EX2001, ¶¶119-120.

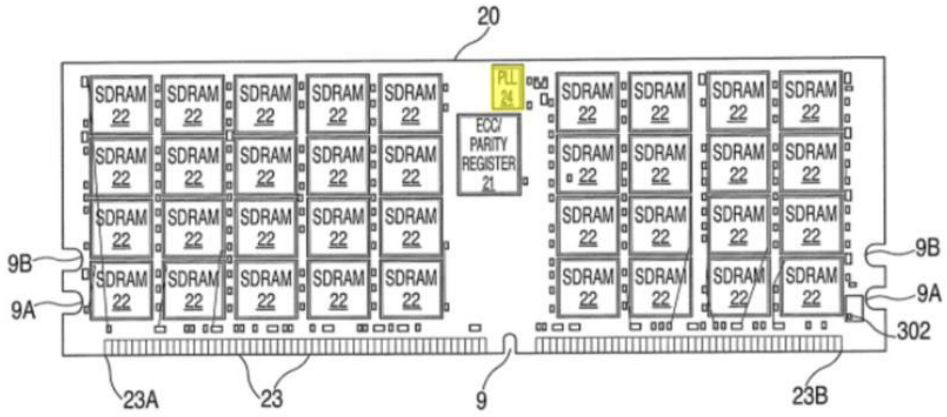
3. The Claims of the '218 Patent Are Not Obvious Over Hazelzet In View of JEDEC Because JEDEC Addresses a Different Memory Architecture and Hazelzet Teaches Away from Using its UE Line for Signaling During Initialization

Petitioner also alleges that POSITA could use Hazelzet's UE line to output JEDEC's alleged training notifications. Pet., 32-33, 54-55. However, as discussed above, Hazelzet expressly teaches away from doing this. Instead, Hazelzet teaches initialization using a separate, distinct bus, like "an IIC bus (such as defined in published JEDEC standards…)." EX1014, [0124]; *id.* [0125] (describing the benefits of doing so, discussed above). Thus, because Hazelzet and JEDEC both include an IIC bus, and *Hazelzet* specifically teaches that JEDEC's IIC bus should be used in *Hazelzet's* architecture for initialization, POSITA would not have been motivated to implement JEDEC's alleged training via Hazelzet's UE line. EX2001, ¶123. JEDEC does not describe any benefit or reason to communicate training status using an open drain output, and therefore, JEDEC does not teach, suggest, or provide a motivation for POSITA to further modify Hazelzet to use Hazelzet's UE output for training during initialization when Hazelzet already discloses, and teaches the benefits of, using a bus during initialization. *See generally* EX1015; EX2001, ¶¶124-125.

In addition, discussed above, Hazelzet's memory modules do not buffer the data lines, which is what would cause the timing issues that JEDEC's training aims to address. EX2001, ¶126. Thus, POSITA would not be motivated to add JEDEC's training to Hazelzet in the first place, let alone trying to perform JEDEC's training in Hazelzet's ECC/Parity register, which is where Hazelzet's UE line resides. EX1014, Figs. 4A & 4B. *Id.* But, *even if* JEDEC's training was added to Hazelzet (as Petitioner contends), instead of completely changing Hazelzet's memory module to fit JEDEC's training, POSITA would have understood that a PLL or DLL component would be the most obvious choice to perform this training:

> Based on various design choices that a POSITA would consider, synchronization circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. The two most common synchronization circuits used are the delay-locked loop (DLL) and the phase-locked loop (PLL). The DLL is widely used in memory interfaces for its simplicity and good jitter performance. An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis.

EX2011, 252; EX2001, ¶126. And because Hazelzet already includes a PLL, that component would be the logical component to perform training—not the ECC/Parity register (that includes the UE line)—without having to completely redesign Hazelzet's memory module. *Id.*



FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A

EX1014, Fig. 4B (annotated).

For at least these additional reasons, POSITA would not have been motivated to implement JEDEC's training on Hazelzet's UE line. EX2001, ¶126.

VIII. The Board Should Invoke Its Discretionary Authority to Deny Institution of the Petition

Institution of *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a); *Harmonic Inc. v. Avid Tech, Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016); *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016).

Here, the Board should exercise its discretion to deny institution because (1) Petitioner has not met its burden of showing that the same or substantially the same art or arguments were not already considered and appropriately rejected by the Office; and (2) little, if any, efficiency will be gained by reviewing the Petition in

parallel with copending litigation, which is unlikely to be stayed, and which thus weighs against instituting these proceedings.

A. The Same or Substantially the Same Art Was Previously Presented to the Office

The Board should exercise its discretion to deny institution under 35 U.S.C. § 325(d) and *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 9 (P.T.A.B. Feb. 13, 2020) (precedential) because Petitioner has not met its burden of showing that the same or substantially the same art and arguments were not already considered and appropriately rejected by the Office with respect to the '218 patent. The Petition contends that the prior IPR Panel (IPR2020-01044) granted institution after having "previously considered extensive evidence that the grounds asserted in this petition are not substantially the same as those before the examiner of the 218 Patent, and that the examiner clearly erred in issuing the 218 Patent." Pet., 16 (citing EX1058, 17-23). This is flatly incorrect. Glaringly, Petitioner can only cite to the prior *Petition* (EX1058)—not the Board's prior Decision Granting Institution (EX1059)—because the Board's prior decision did not consider whether Petitioner's grounds, or any other grounds, are substantially the same as those that were before the examiner. *See generally* EX1059; *id.*, 8-18 (considering discretionary denial only under 35 U.S.C. § 314(a) in view of parallel district court litigation). The Board's prior decision did not address whether

Petitioner's grounds are the same or substantially the same art and arguments that were already considered and appropriately rejected by the examiner with respect to the '218 Patent, and Petitioner cannot meet its burden under § 325(d) here by attempting to incorporate by reference the prior petition, as it appears to have tried to do. *Prollenium US Inc. v. Allergan Industrie*, No. IPR2019-01505, 2020 WL 1322827, at *8 (P.T.A.B. Mar. 19, 2020) ("As noted at page 35 of our Consolidated Trial Practice Guide … , '§ 42.6(a)(3) prohibits incorporating arguments by reference from one document into another.'"). Petitioner has the burden to establish why the art and proposed grounds present something new and failed to do so. Institution should be denied as a result.

As an additional, separate reason for the Board to exercise its discretion to deny institution under § 325(d) and *Advanced Bionics*, as discussed in Patent Owner's Preliminary Response in IPR2022-00064 (filed concurrently herewith), Petitioner has not met its burden of showing that the same or substantially the same art and arguments were not already considered and appropriately rejected by the Office with respect to US Patent No. 10,474,595 (a continuation application of the '218 patent), where three of the four references relied on in this Petition were expressly considered. Specifically, Hazelzet, Buchmann, and Kim are all cited on the face of the '595 Patent. Moreover, the combinations of Hazelzet and Buchmann and Hazelzet, Buchman, and Kim were discussed extensively in *SK Hynix Inc. v.*

Netlist, Inc., IPR2018-00303, Final Written Decision, Paper 42 (PTAB March 21, 2019) and other filings in IPR2018-00303, which the Office also considered before allowing the '595 Patent claims. EX2021, 3–4. Because the claims of the '218 are materially similar to the claims of the '595 Patent, the Board should likewise exercise its discretion to deny institution with respect to the '218 Patent.

The Petition fails to meet its burden to establish why the art and proposed grounds present something new, and ignores that the art and arguments presented were expressly considered in a related application that issued as the '595 patent. Petitioner's argument that "the Board previously instituted trial in IPR2020-01044 on the same grounds asserted in this petition" (Pet., 16) does not save the deficiencies of this Petition. As discussed throughout this Preliminary Response, *this Petition* presents new arguments that demonstrate both the inoperability of the proposed combinations and the Petition's hindsight reconstruction of the '218 patent claims, and *this Preliminary Response* presents evidence and arguments not presented to or considered by the Board during that prior institution decision. The Petition fails under § 325(d) and *Advanced Bionics*; institution should be denied as a result.

B. The Fintiv Factors Also Weigh Against Institution

Although the framework set forth in *Apple, Inc. v. Fintiv, Inc.*, 2020 WL 2126495, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) typically applies to cases with parallel invalidity defenses, the factors ultimately "relate to whether

efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding." *Fintiv, Inc.*, 2020 WL 2126495 at *3.

In exercising its discretion in view of a trial date, the Board evaluates six "*Fintiv* factors." *Id.* In doing so, "the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Id.*, 6. Patent Owner addresses each factor in turn.

Factor (1): Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted. Here, the parallel patent proceeding between the parties was initiated by the Petitioner, not the Patent Owner. *See* EX1054 (*Samsung Elecs. Co., Ltd. v. Netlist, Inc*., No. 21-CV-1453, Dkt. 1 (D. Del. Oct. 15, 2021)). Critically, in that proceeding Petitioner seeks declarations of non-infringement of four patents, one of which it did not even petition for an IPR until *this week*. This makes it unlikely that institution of this Petition will result in a stay at this stage or avoidance of any parallel litigation (and no stay has been issued or sought). Given that institution will not likely presently save judicial or party resources in the parallel action, this factor weights against institution.

Factor (2): Proximity of the court's trial date to the Board's projected statutory deadline for a final written decision. The district of Delaware has not yet set a trial date, so this factor is neutral.

Factor (3): Investment in the parallel proceeding by the court and the parties. The parties have invested in pleading and motion practice in the parallel proceeding, although claim construction and merits determinations have not been reached. Accordingly, this factor is neutral or marginally against institution.

Factor (4): Overlap between issues raised in the petition and in the parallel proceeding. Petitioner does not challenge the validity of the '218 Patent in the parallel proceedings, and that proceeding involves a patent for which Petitioner only sought an IPR this week. Thus, while that proceeding may render the need for this IPR moot, the opposite is not likely true—this IPR does not stand to obviate the need for the parallel action to proceed. As such, this factor also weighs against institution.

Factor (5): Whether the petitioner and the defendant in the parallel proceeding are the same party. The parties in the parallel proceeding are the same, thus this factor also weighs against institution.

Factor (6): Other circumstances that impact the Board's exercise of discretion, including the merits. Alternatively, the Board may consider under the "other circumstances" factor that the Petitioner here has not met its burden of showing that the asserted prior art and/or arguments were not already considered by the Office in the '218 Patent's prosecution, much less demonstrated a material error by the Office. Accordingly, this factor weighs against institution.

In sum, the majority of the *Fintiv* factors weigh against institution. Accordingly, the Board should exercise its discretion to deny institution.

IX. Conclusion

For the foregoing reasons, Patent Owner respectfully submits that the Board should deny institution of this Petition.

Date: February 18, 2022

Respectfully submitted,

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Certificate of Word Count

The undersigned hereby certifies that the portions of the above-captioned **NETLIST, INC.'S PATENT OWNER'S PRELIMINARY RESPONSE** specified in 37 C.F.R. § 42.24 has 13,450 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word 2016.

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Certificate of Service

A copy of **NETLIST, INC.'S PATENT OWNER'S PRELIMINARY RESPONSE**, together with the referenced and submitted exhibits (Exhibits 2001-2021), was served via electronic mail on the following counsel of record for Petitioner at the email address DLSamsungNetlistIPRs@BakerBotts.com as indicated in the Petition for electronic service to the following Petitioner counsel:

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